Rishikesh Singh

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Embedded Systems Engineer | SoC Architecture | Power & Performance Optimization

Embedded Systems Engineer with 5+ years of experience in ARM-based multicore SoCs, specializing in performance characterization, power modelling and optimization, architectural analysis, and performance-per-watt optimization. Experienced in workload-driven analysis of CPU, memory hierarchy and NoC subsystems, DVFS, PVT characterization, power modes, and system-level bottleneck identification. Hands-on experience developing C-based characterization frameworks and power/performance calculators, and working with SoC architecture and design teams to evaluate architectural tradeoffs.

Experience

Systems & Applications Engineering — **NXP Semiconductors** — *Noida, India* — **07/2021 – Present**

Lead Systems & Applications Engineer, G2L — 04/2025 - Present

- Developed a bare-metal real-time power monitoring utility to measure voltage, current, and total power across SoC rails using on-board current monitors, enabling power budgeting and workload-level power characterization per power rail.
- Applied the power measurement utility to AI workloads, correlating DRAM, core, and AI accelerator power consumption with inference throughput to derive Inference-per-Second-per-Watt (IPS/W) metrics for performance-per-watt optimization and competitive analysis.
- Profiled CPU, memory, cache, and NoC subsystems using CoreMark-Pro, LMbench, and internal workloads across runtime, standby, and low-power operating modes, identifying architectural bottlenecks and thus driving optimization recommendations.
- Developed and implemented Dynamic Voltage and Frequency Scaling (DVS & DVFS) algorithms, analyzing the performance, voltage, and frequency trade-offs to optimize system-level power efficiency (Performance-per-Watt, DMIPS/W).
- Developed a C-based performance characterization framework for memory hierarchy to evaluate TCMs, Cache, SRAM, DRAM and NVMs, enabling quantitative analysis of memory subsystem behavior and its impact on system performance.
- Worked with SoC Design and Systems Architecture teams on the Power and Reset architecture for next-generation automotive processors, evaluating power domains, sequencing, operating modes, and system-level requirements.
- Represented NXP through the University Outreach Program (NXP Campus Connect), delivering technical sessions on SOC architecture, Automotive SOC technologies, and embedded systems.

Senior Systems & Applications Engineer, G2 — 04/ 2023 - 04/2025

- Supported system power architecture and power optimization for various customer programs using NXP VR5510 and PF53 PMICs by developing optimized power-tree topologies and reducing runtime and standby power.
- Analyzed SoC power requirements across operating modes and workloads, providing recommendations for power-domain configuration, voltage rails, sequencing, and PMIC settings to improve system-level power efficiency.
- Led silicon bring-up of ARM-based 5nm multicore automotive SoCs, performing HW/SW debug and subsystem characterization to understand silicon behavior, performance, and power characteristics.
- Worked with SoC Architecture and Design teams to analyze boot stages, initialization, and power-state behavior, optimizing bootloader configurations and platform initialization flows to meet critical customer KPIs for power-up and boot time.
- Performed hardware schematic reviews for customer platforms, evaluating power delivery, reset, clocking, and SoC interfaces and identifying issues prior to production.
- Developed customer-facing SoC Dynamic & Total Power Calculators, SoC Boot Process, Hardware Design Guides, and Engineering Bulletins to communicate power requirements, system architecture considerations, and recommended implementation guidelines.
- Developed and debugged Linux boot flows on ARM-based automotive processors, enabling boot from eMMC, UFS and SD storage devices through bootloader configuration, platform initialization and storage subsystem validation.
- Developed low-level validation and diagnostic software in C for PCIe, eMMC, SD and Flash subsystems during first-silicon bring-up of S32N55 and S32N79 automotive processors.

Systems & Applications Engineer, G1 — 07/ 2021 - 04/2023

- Optimized and executed single & multi–Core Benchmarks, e.g. Dhrystone, CoreMark, and CoreMark-Pro for NXP's S32G and S32N Family of Automotive Processors. Optimized the Memory Hierarchy to achieve a performance increase of >15%.
- Supported customer queries on varying topics related to NXP's HW and SW products through NXP Community, meeting all the critical KPIs (low average resolution time and near zero escalation rates).
- Owned and published the Errata Reports for S32G2 and S32G3 family of processors, providing comprehensive customer notification for any potential functional deviation of the SOC.
- Represented NXP in various technical forums for presenting the NXP's latest technological breakthroughs and products to customers.

Education

Bachelor of Technology — **National Institute of Technology, Warangal** — *Warangal, India* — **07/2017 - 06/2021**

- Major in Electrical and Electronics Engineering, **GPA: 7.49/10**
- **Thesis Project** – Effect of Zero Vector Placement in an Inverter Fed Induction Motor Drive

Intermediate — **Heliger Borden Education Center, Kanpur** — *Kanpur, India* — **07/2014 - 06/2016**

- Class XII – ISC Board
- Aggregate Score – 95.6%

Skills

- SoC Architecture | Performance Analysis | Power Architecture | AI-Inference/Sec/W and Performance-per-Watt Optimization
- Power Management | DVFS | Power Domains & States | Runtime & Standby Power
- Performance Benchmarks & Modelling | Workload Analysis | System Bottleneck Analysis
- Boot Architecture | Secure-Boot Flow Design | BootROM and Bootloaders | ARM Processors (Cortex M/R/A)
- Embedded C/C++, Python, Bash **|** EB Tresos (AUTOSAR), Software Integration, Validation, RCA, and tool-based configuration
- HW Schematics Reviews **|** System-level Debugging (HW/SW, LTB/TPIU Tracing, S32 Debug Probe) | Board/Si Bring-up
- AI-Assisted Development and Debugging | Copilot, ChatGPT, Claude etc.